trench fill allows the source contact metallization to be designed for maximum contact area without concern for inadvertent oxide etch, since there is not exposed oxide in the trench fill. For shallow trenches, accurate planarization is more readily achieved when working with a homogeneous surface, as opposed to a heterogeneous polysilicon/oxide surface. In addition, the homogeneous polysilicon surface may be etched (e.g., wet HF or plasma) prior to metallization without damaging exposed oxide dielectric.

FIG. **4** shows a flow chart **400** for a method embodiment of the present claimed invention. This fabrication method applies to a trench in a silicon substrate such as that shown in FIG. **2**A. In step **405**, an oxide coating is formed on the trench wall and bottom, as shown in FIG. **2**B. In step **410**, the oxide coating is etched back to expose the upper portion of the trench wall. This may be done by low angle ion milling of the substrate under rotation, or other process. In step **415**, polysilicon is deposited to completely fill the trench. This typically will involve an overfill. In step **420** the excess polysilicon is removed to level the polysilicon fill with surface of the substrate. This may be done by etching, chemical mechanical polishing (CMP) or other process.

FIG. **5** shows a flow chart for a method embodiment of the present claimed invention using discrete polysilicon depositions. The method shown FIG. **5** is more involved than the method shown in FIG. **4**; however, the more involved method provides better dimension control.

In step **505**, a first oxide coating is formed on a silicon substrate. The first oxide coating may be thermally grown, or it may be deposited by chemical vapor deposition (CVD) or other deposition process.

In step **510**, a first polysilicon coating is formed on top of the first oxide coating. This coating is preferably formed using CVD.

In step **515**, a trench is etched into the silicon substrate through the first oxide coating and the first polysilicon coating. The result of this step is shown in FIG. **2**A.

In step **520**, a second oxide coating is formed on the surface of the substrate and on the wall and bottom of the trench, as shown in FIG. **2**B.

In step **525**, a second polysilicon coating is formed on the first oxide coating, filling the remainder of the trench. This step is preferably done by CVD and may involve a degree of overfill.

In step **530**, the excess polysilicon from the second polysilicon coating is removed to create a first polysilicon fill that is nominally level with the surface of the substrate as shown in FIG. **2**C. This step is preferably done with a reactive ion etch.

In step **535**, a portion of the first oxide coating is etched back below the surface of the substrate to create a gap between the silicon substrate and the first polysilicon fill. This etch effectively creates a "moat" around the first polysilicon fill with a depth D as shown in FIG. **2**D. Depth D is preferably less than 5000 angstroms.

In step **540**, a third polysilicon coating is formed to fill the gap (moat) between the silicon substrate and the first polysilicon fill. This step is preferably done by CVD and may involve a degree of overfill.

In step **545**, the excess polysilicon from the third polysilicon coating is removed to create a second polysilicon fill that is nominally level with the surface of the substrate as shown in FIG. **2**C. This step is preferably done with a reactive ion etch as shown by the structure of FIG. **2**E; however, mechanical polishing or CMP may be used to fully planarize the surface.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

What is claimed is:

1. An electronic silicon device comprising:
- a silicon substrate comprising a planar surface;
- a trench disposed in said planar surface of said silicon substrate, said trench comprising a wall and a bottom;
- a silicon dioxide layer disposed on the bottom of said trench and also on a first portion of said wall, said layer being terminated at a distance D below said planar surface of said silicon device;
- a polysilicon fill disposed on the surface of said silicon dioxide layer and on a second portion of said wall; and
- a metallization disposed on the planar surface of said silicon substrate and an upper surface of said polysilicon fill.

2. The electronic silicon device of claim **1**, wherein the upper surface of said polysilicon fill is approximately level with or above said planar surface of said silicon substrate.

3. The electronic silicon device of claim **1**, further comprising a junction field effect transistor (JFET).

4. The electronic silicon device of claim **1**, further comprising an integrated circuit.

5. The electronic silicon device of claim **1**, wherein said trench is disposed above a gate.

6. The electronic silicon device of claim **1**, wherein said trench is disposed adjacent to a source.

7. The electronic silicon device of claim **1**, wherein said silicon dioxide layer is between 100 angstroms and 3000 angstroms in thickness.

8. The electronic silicon device of claim **1**, wherein said silicon dioxide layer is thermally grown.

9. The electronic silicon device of claim **1**, wherein said silicon dioxide layer is deposited.

10. A semiconductor device comprising:
- a silicon substrate;
- a trench disposed in said silicon substrate, said trench comprising a wall and a bottom;
- a silicon dioxide layer disposed on the bottom of said trench and also on a first portion of said wall, said layer being terminated below an original surface of said silicon substrate;
- a polysilicon fill disposed on the surface of said silicon dioxide layer and on a second portion of said wall; and
- a metallization disposed on the original surface of said silicon substrate and an upper surface of said polysilicon fill.

11. The semiconductor device of claim **10**, wherein said polysilicon fill comprises an upper surface that is disposed between a top surface of said silicon dioxide layer and said original surface of said silicon substrate.

12. The semiconductor device of claim **10**, further comprising a junction field effect transistor (JFET).

13. The semiconductor device of claim **10**, further comprising an integrated circuit.